oxygen gas as a reactive gas, at a heat treatment temperature of, for example, not less than 700° C. and not more than 1000° C.

As a result of the thermal etching, trench TR is formed as shown in FIG. **11**. During the formation of trench TR, epitaxial substrate **100** is etched in a side etching manner from the opening of mask **247** as indicated by an arrow SE. Further, during this thermal etching, a special plane is spontaneously formed on side wall surface SW of trench TR, in particular, on its portion formed of p type body layer **122**.

It should be noted that the reactive gas may contain a carrier gas in addition to the chlorine gas and the oxygen gas. An exemplary, usable carrier gas is nitrogen (N_2) gas, argon gas, helium gas, or the like. When the heat treatment temperature is set at not less than 700° C. and not more than 1000° C. as described above, a rate of etching SiC is, for example, approximately 70 μm/hour. Moreover, in this case, mask **247**, which is made of silicon oxide and therefore has a very large selection ratio relative to SiC, is not substantially etched during the etching of SiC.

As shown in FIG. **12**, a silicon film **90** is formed on epitaxial substrate **100** having mask **247** provided thereon. In other words, silicon film **90** is formed while using mask **247**. Silicon film **90** covers bottom surface BT of trench TR. In the present embodiment, silicon film **90** also covers p type body layer **122** on side wall surface SW.

Silicon film **90** has a first thickness UB on bottom surface BT. Silicon film **90** has a second thickness UA on side wall surface SW formed of p type body layer **122**. Side wall surface SW formed of p type body layer **122** is not directly covered with mask **247**, but is located in the shadow of mask **247** during the formation of silicon film **90**. Therefore, second thickness UA is smaller than first thickness UB. Conversely, first thickness UB is larger than second thickness UA. The silicon film is preferably made substantially only of silicon, but may be made of silicon containing an impurity.

Next, mask **247** is removed with an appropriate method such as etching (FIG. **13**). In doing so, the portion of silicon film **90** on mask **247** is also removed.

Next, a portion of silicon film **90** is removed such that silicon film **90** remains on bottom surface BT of trench TR and p type body layer **122** is exposed at side wall surface SW of trench TR. Specifically, the following steps are performed.

First, silicon film **90** (FIG. **13**) is thermally oxidized such that the oxidation progresses to a thickness smaller than first thickness UB (FIG. **12**) and larger than second thickness UA (FIG. **12**). This thermal oxidation is preferably performed at a temperature at which silicon is thermally oxidized and silicon carbide is not substantially thermally oxidized. Consequently, on side wall surface SW, silicon film **90** having second thickness UA is oxidized as shown in FIG. **14**. On bottom surface BT, a portion corresponding to second thickness UA of silicon film **90** having first thickness UB (FIG. **13**) is oxidized to become a silicon oxide film **90**A, and the remaining portion remains as a silicon film **90**B. The entire portion of silicon film **90** that was located on side wall surface SW formed of p type body layer **122** becomes silicon oxide film **90**A. The portion of silicon film **90** that was located on bottom surface BT partially becomes silicon oxide film **90**A on the surface side, and silicon film **90**B remains between silicon oxide film **90**A and bottom surface BT. This thermal oxidation is performed, for example, at not less than 800° C. and not more than 950° C. Next, silicon oxide film **90**A is removed by etching (FIG. **15**). This removal can be performed, for example, by wet etching using hydrofluoric acid.

In the manner described above, a portion of silicon film **90** (FIG. **13**) is removed such that silicon film **90** (i.e., silicon film **90**B) remains on bottom surface BT of trench TR and p type body layer **122** is exposed at side wall surface SW of trench TR.

Next, oxidation is performed in trench TR, thereby forming gate oxide film **201** (FIG. **1**) on the inner surface of trench TR. Specifically, the following steps are performed.

First, silicon film **90**B (FIG. **15**) is thermally oxidized. Thus, second portion **201**B that forms a portion of gate oxide film **201** (FIG. **1**) is formed (FIG. **16**). Silicon film **90**B is thermally oxidized, for example, at not less than 800° C. and not more than 950° C. Next, as shown in FIG. **17**, epitaxial substrate **100** made of silicon carbide is thermally oxidized, thereby forming first portion **201**A of gate oxide film **201**. Epitaxial substrate **100** is thermally oxidized preferably at a temperature higher than the temperature at which silicon film **90**B is thermally oxidized, for example, is thermally oxidized at not less than 1300° C.

Gate oxide film **201** is formed in the manner described above.

As shown in FIG. **18**, gate electrode **202** is formed on gate oxide film **201**. In the present embodiment, gate electrode **202** is formed in direct contact with first portion **201**A on p type body layer **122**. A method for forming gate electrode **202** can be performed, for example, by forming a film of conductor or doped polysilicon and performing CMP (Chemical Mechanical Polishing).

As shown in FIG. **19**, interlayer insulating film **203** is formed on gate electrode **202** and gate oxide film **201** so as to cover the exposed surface of gate electrode **202**.

Referring to FIG. **20**, etching is performed to form openings in interlayer insulating film **203** and gate oxide film **201**. Through the opening, each of n region **123** and contact region **124** is exposed on the upper surface of the mesa structure. Next, on the upper surface of the mesa structure, source electrode **221** is formed in contact with each of n region **123** and contact region **124**.

Referring to FIG. **1** again, source interconnection **222**, drain electrode **211**, and protecting electrode **212** are formed. In this way, MOSFET **500** is obtained.

According to MOSFET **500** (FIG. **1**) of the present embodiment, gate oxide film **201** includes first portion **201**A formed by the oxidation of epitaxial substrate **100**, as well as second portion **201**B formed by the oxidation of silicon film **90** on bottom surface BT of trench TR. Thus, the thickness of gate oxide film **201** on bottom surface BT of trench TR can be increased for the thickness of second portion **201**B. That is, the thickness of a portion of the gate oxide film where breakdown particularly tends to occur can be increased. Accordingly, MOSFET **500** can have a high breakdown voltage.

Moreover, epitaxial substrate **100** is etched in a side etching manner from the opening of mask **247** (arrow SE in FIG. **11**). That is, side wall surface SW of trench TR is recessed by the side etching. As a result, mask **247** remains protruding from side wall surface SW. During the formation of silicon film **90** using mask **247**, therefore, silicon film **90** is unlikely to be formed on side wall surface SW since side wall surface SW is located in the shadow of mask **247**.

Moreover, the step of forming silicon film **90** is performed using mask **247** (FIG. **12**). Thus, the formation of silicon film **90** on the portion covered with mask **247** can be prevented.